WHAT IS CLAIMED IS:

1. A circuit arrangement for detecting a received signal, comprising:

a rectifier having an input adapted to have a received signal applied thereto and having an output adapted to provide a rectified signal;

a signal capacitor connected to said output of said rectifier;

a signal evaluating circuit connected to said signal capacitor; and

a discharge current sink that is connected to said signal capacitor and that comprises a current mirror circuit comprising plural transistors circuit-connected with one another in a cascode arrangement.

2. The circuit arrangement according to claim 1, further comprising a receiving antenna connected to said input of said rectifier.

3. The circuit arrangement according to claim 1, wherein said transistors are MOSFET transistors.

4. The circuit arrangement according to claim 1, wherein said current mirror circuit includes a total of exactly five of said transistors.

5. The circuit arrangement according to claim 4, wherein said cascode arrangement of said five transistors includes a discharge current path having two of said transistors connected across said signal capacitor, a first reference current path having two of said transistors, and a second reference current path having one of said transistors.

6. The circuit arrangement according to claim 1, wherein said current mirror circuit is a cascode current mirror circuit having a wide-swing output.

7. The circuit arrangement according to claim 1, further comprising a voltage limiter circuit connected to said signal capacitor.

8. The circuit arrangement according to claim 7, wherein said voltage limiter circuit comprises series-connected diodes that are connected parallel to said signal capacitor.

9. The circuit arrangement according to claim 7, wherein said voltage limiter circuit comprises a zener diode connected parallel to said signal capacitor.

10. The circuit arrangement according to claim 7, wherein said output of said rectifier includes two output poles, and wherein said signal capacitor, said discharge current sink, said voltage limiter circuit, and said signal evaluating

circuit are all connected parallel to each other between said two output poles of said rectifier.

11. The circuit arrangement according to claim 1, wherein said output of said rectifier includes two output poles, and wherein said signal capacitor, said discharge current sink and said signal evaluating circuit are all connected parallel to each other between said two output poles of said rectifier.

12. The circuit arrangement according to claim 1, wherein said discharge current sink exhibits a current-voltage characteristic having a linear range with decreasing current for increasing voltage.

13. The circuit arrangement according to claim 1, wherein said discharge current sink exhibits a current-voltage characteristic having a range in which a discharge current flowing through said discharge current sink is substantially independent of a signal voltage prevailing on said signal capacitor.

14. The circuit arrangement according to claim 1, integrated in a passive or semi-passive transponder.